



REPLACEMENT SHEET
1/7

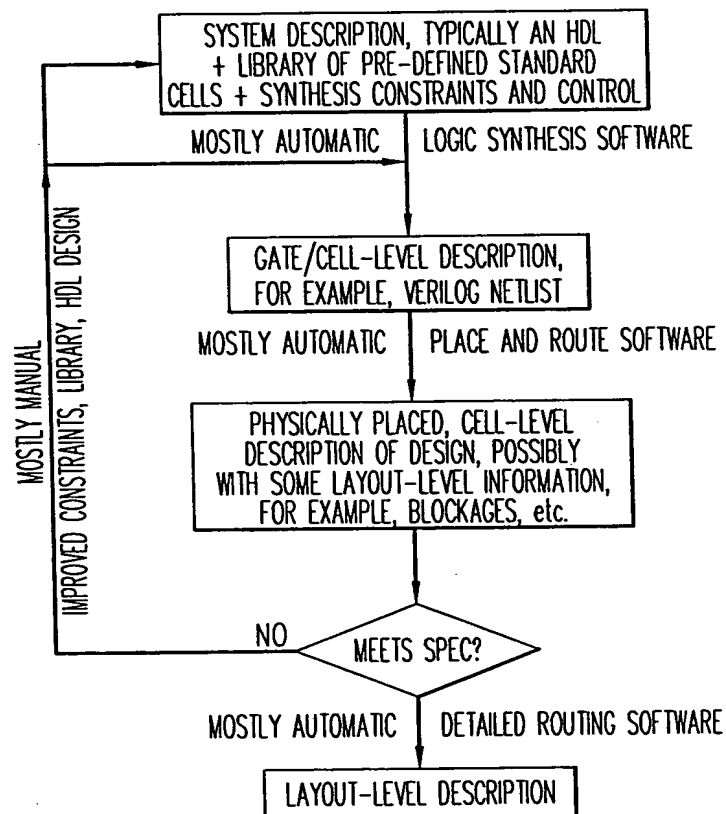
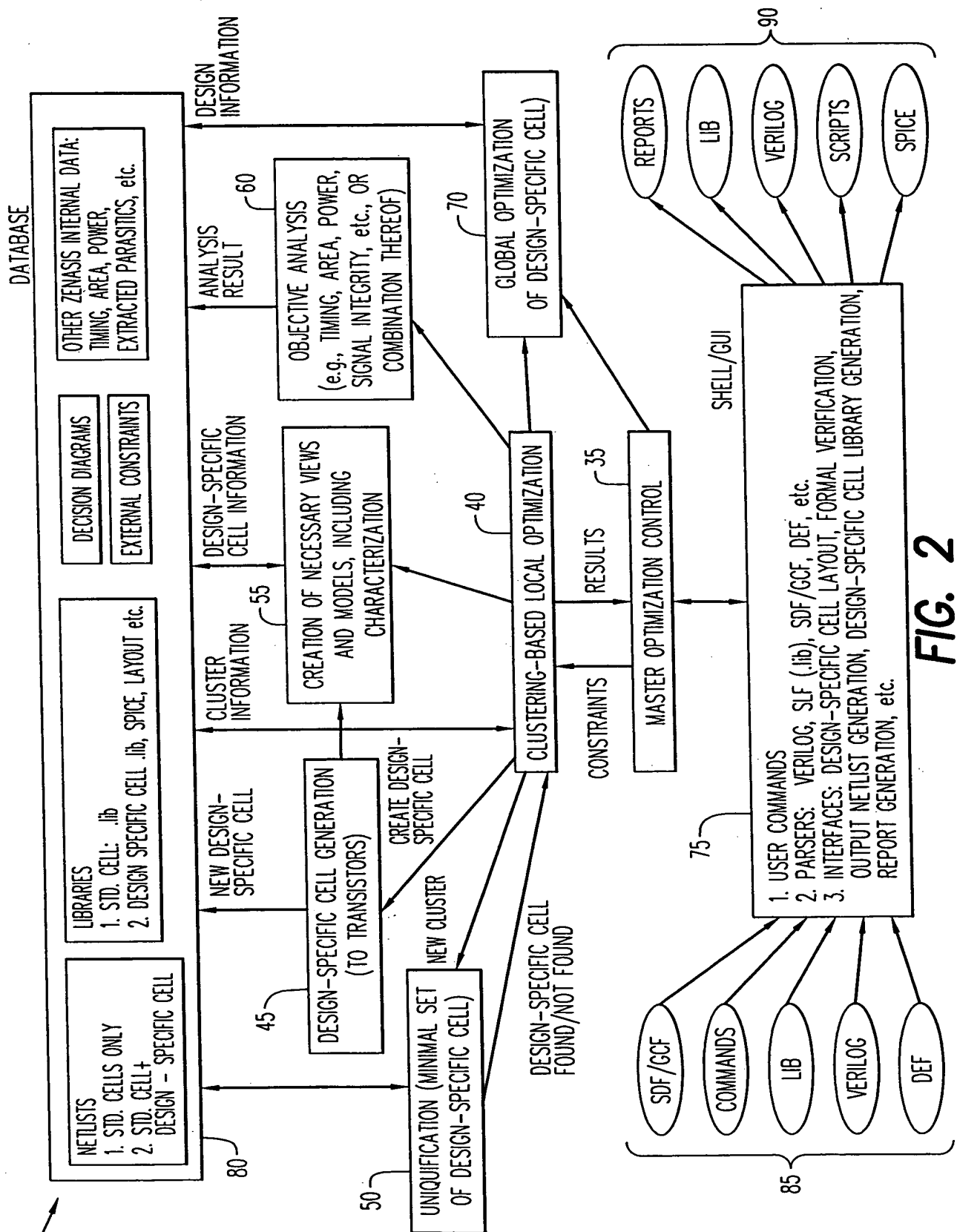


FIG. 1



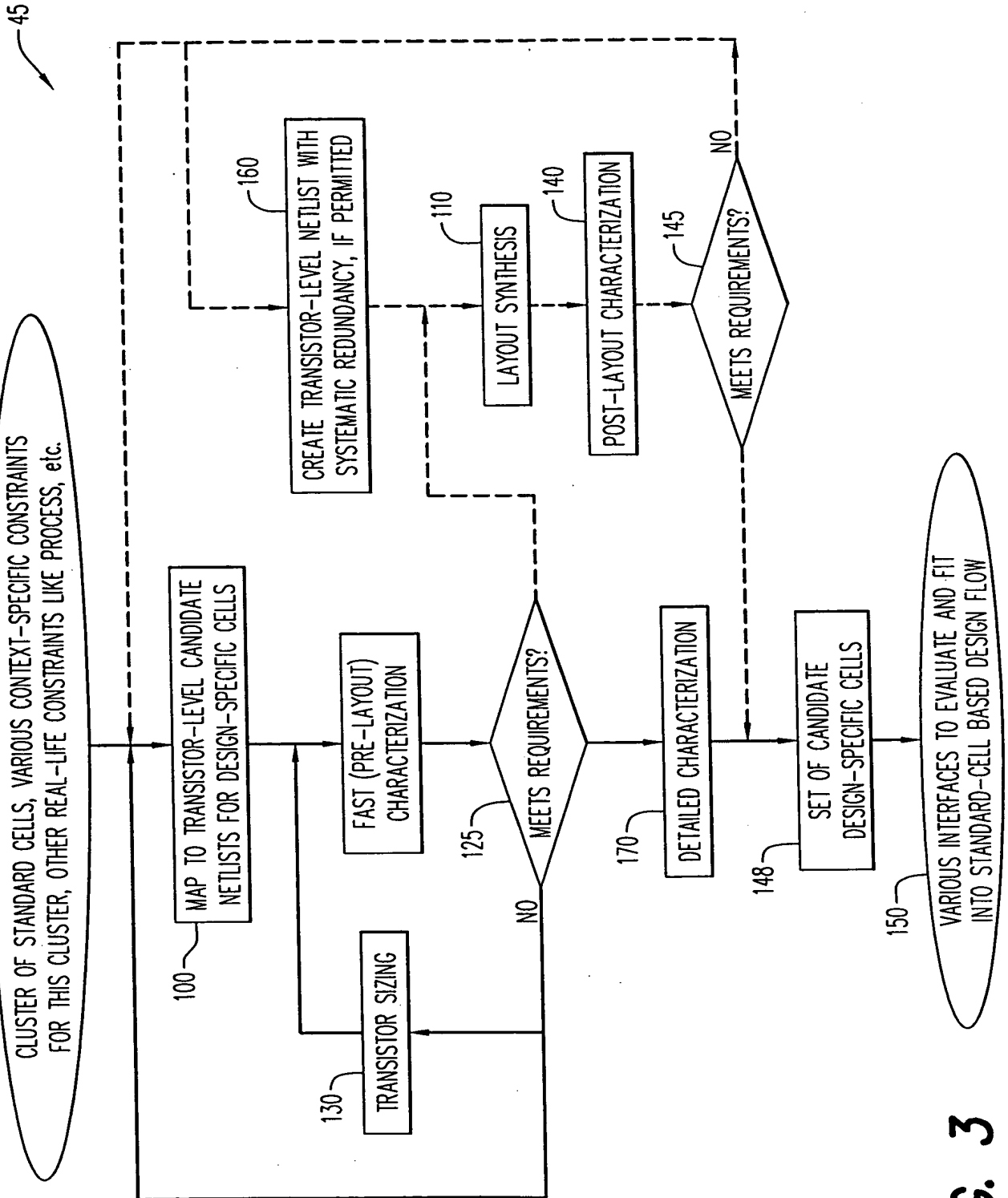


FIG. 3

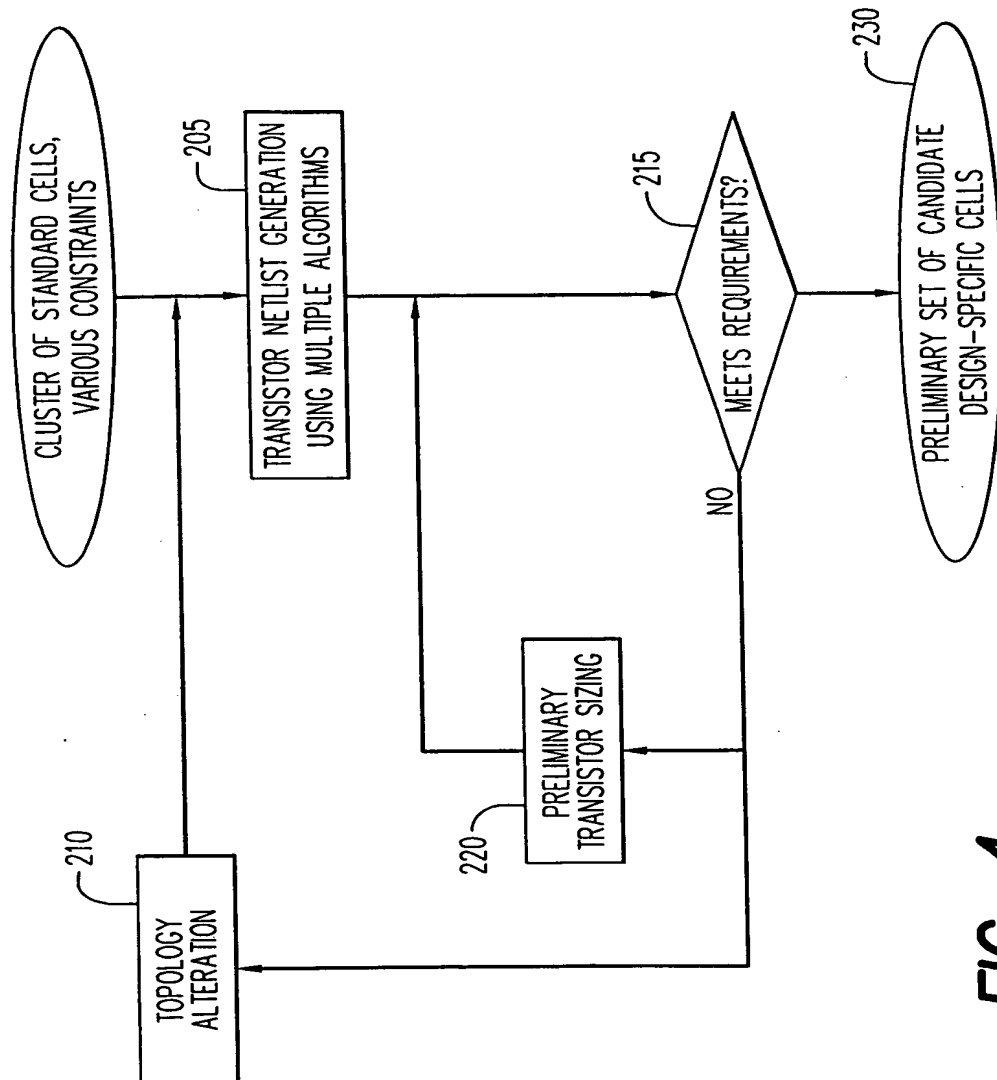


FIG. 4

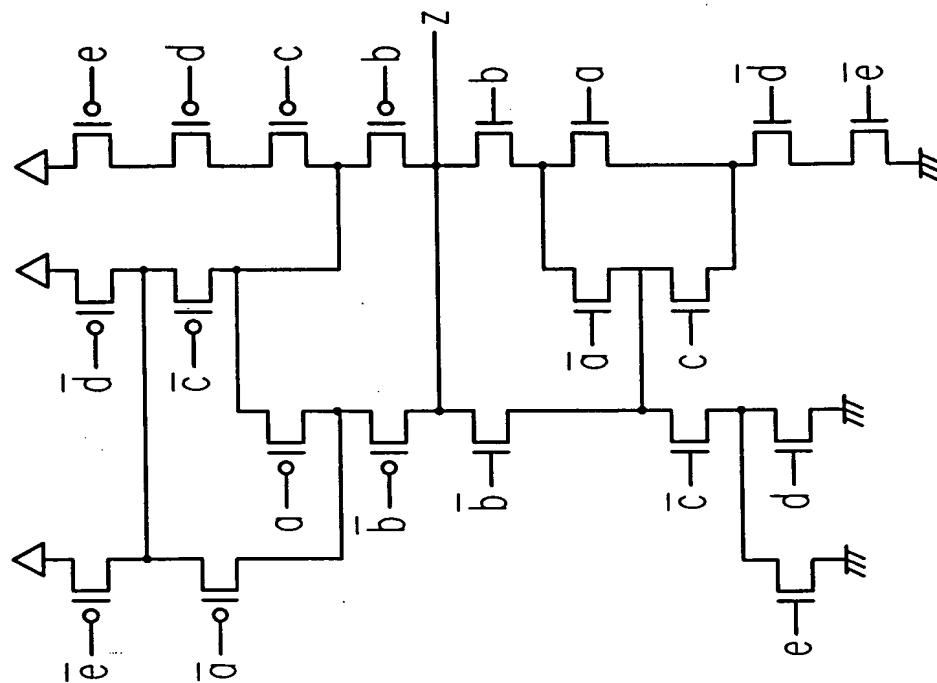


FIG. 5b

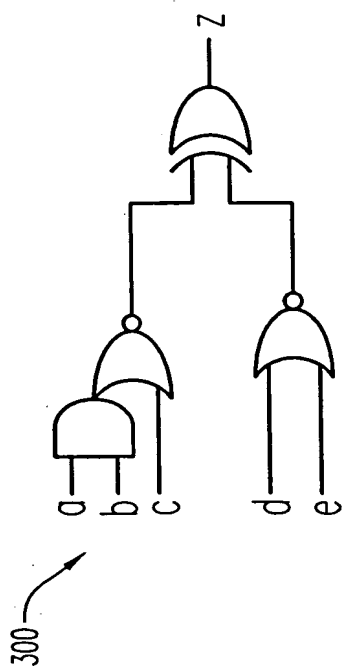


FIG. 5a

CRITICAL PATH TO z THROUGH b

⇒ DELAY FROM b TO z : 0.33 ns

⇒ DESIGN-SPECIFIC CELL DELAY : 0.14 ns

FIG. 5c

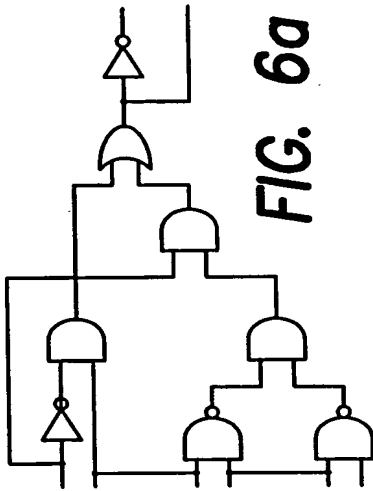


FIG. 6a

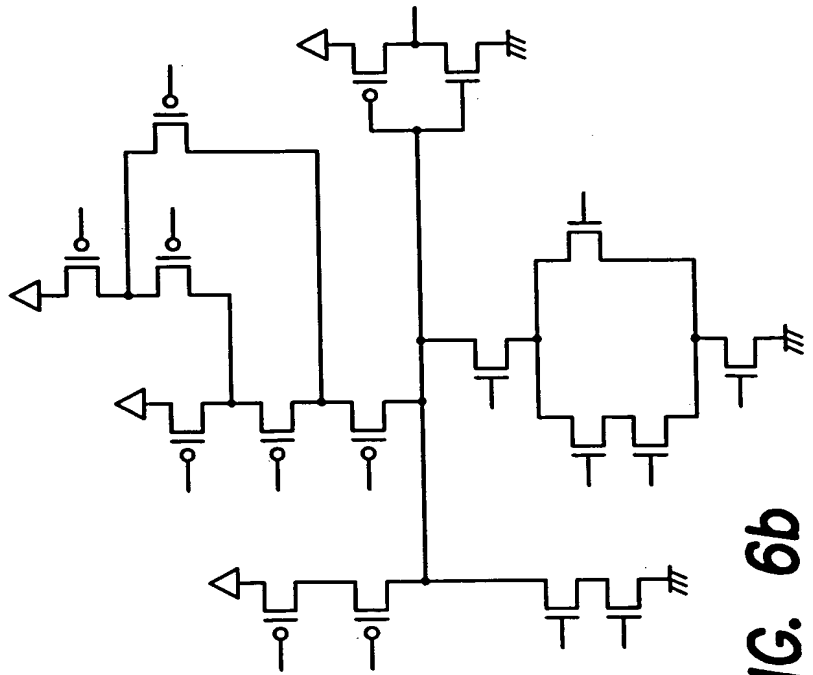


FIG. 6b

CRITERIA	ORIGINAL	OPTIMIZED
# OF CELLS	8	1
# OF TRANSISTORS	32	17
# OF WIRES (INCL. I/O)	12	5

FIG. 6c

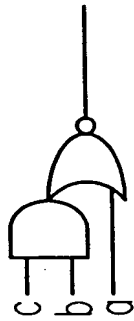


FIG. 7a

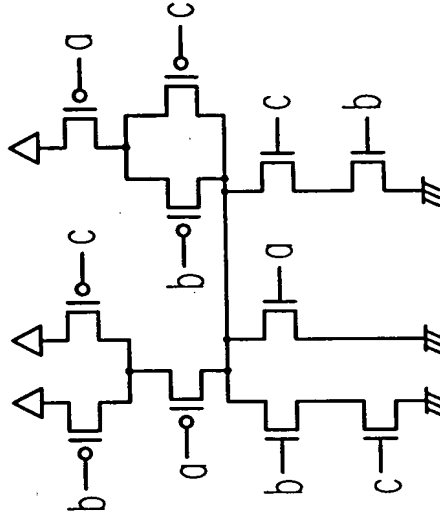


FIG. 7c

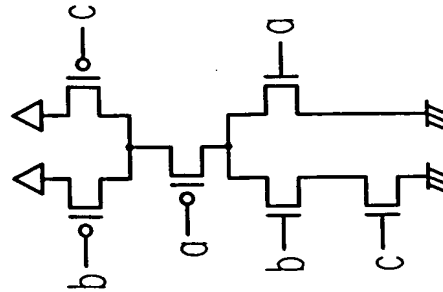


FIG. 7b